Amendments to the Specification:

Please replace the paragraph beginning on page 8, line 10, with the following amended paragraph:

FIG. 5 shows an embodiment of the propagation delay detection circuit 401, sampling the signal transition of a connection of address and data bus 407 and that of connection device 409. The propagation delay detection circuit comprises a fine-tuned delay matcher 501 and a mutual exclusion element 503, and it arbitrates between the two received signals, i.e. the reference signal corresponding to connection device 409 and the actual signal corresponding to data bus 407. In case a probe is present to monitor the data bus 407, the actual signal is delayed when compared to the reference signal and as a result the mutual exclusion element 503 allows the reference signal to propagate, setting the alert signal 411. In case no probe is present, the actual signal should be allowed to propagate, in case of which the alert signal 411 is not set. In order to take natural variations in the transition of the actual signal into account, the dummy signal is delayed by the fine-tuned delay matcher 501. The fine-tuned delay matcher 501 delays the dummy signal such that for normal variations in ~~de delay~~ delay of the actual signal no alert signal is generated, whereas in other cases an alert signal is generated.

Please replace the paragraph beginning on page 9, line 4, with the following amended paragraph:

In a further alternative embodiment, a propagation delay circuit may be coupled to connection device between different units of the electronic device in order to prevent the retrieval of secret information from the device. Referring to FIG. 1, a propagation delay circuit is coupled to ~~connection~~ a connection device between the cache controller CC and the data cache DC, for example. Alternatively, propagation delay circuits may be coupled to connection devices between more than one pair of units, for example one coupled to the connection device between the cache controller CC and the instruction

cache IC, as well one coupled to the connection device between the core pipeline CP and the coprocessor COP.